REMARKS

Claims 10, 11, 15, 16, 18 – 20 are pending. In the above-identified Office Action, the Examiner rejected Claims 10, 11, 15, 16, 18 – 20 under 35 U.S.C. § 102(b) as being anticipated by Bruce *et al.* (U.S. Patent No. 6,000,006) hereinafter 'Bruce'.

On receipt of the Office Action, Applicant's Attorney (William J. Benman) conducted a telephonic interview with the Examiner on May 9, 2007. During the interview, Mr. Benman and Examiner Flournoy discussed the Claims and the rejection thereof based on Bruce. No agreement was reached. However, the Examiner suggested that the appropriate course of action would be for Applicant to submit an Amendment After Final. Accordingly, the present paper is submitted as an Amendment After Final.

For the reasons set forth below, the present Application is believed to be in proper form for allowance. Reconsideration allowance and passage to issue are respectfully requested.

As stated previously, the present invention addresses the need in the art for a system or method for reducing average access times of slow memory technologies. In accordance with the invention, a system and method are taught for storing read and/or write pointer addresses in a buffer prior to power down. This data is used to provide for a rapid recovery on a reapplication of power so that processes may be resumed at the locations at which the processes were terminated. The inventive system discloses and claims a device with a processor programmed to cause a memory interface **to store memory addresses** that have been recently access **on the issuance of a power down command**.

The invention is set forth in Claims of varying scope of which Claim 15 is illustrative. Claim 15, as previously presented, recites:

> 15. A digital device that comprises:
> a memory having a **buffered memory interface** with one or more read buffers; and
> a processor coupled to the memory device and configured to retrieve stored information from the memory, **said processor being programmed to cause the memory to receive a power down command before electrical power is removed** from the memory **and the buffered memory interface to responsively store**, in a nonvolatile memory, **one or more addresses of memory locations that have been recently accessed.** (Emphasis added.)

None of the references teach, disclose or suggest the invention as presently claimed. That is, none of the references teach, disclose or suggest a device with a processor programmed to cause a memory interface **to store memory addresses** that have been recently access **on the issuance of a power down command.**

In the above-identified Office Action, the Examiner relied on Bruce in the rejection of the Claims. Bruce purports to show a system for wear-leveling non-volatile flash RAM mass storage. As to Claim 15, the Examiner suggested that at column 13, lines 31 – 34, Bruce teaches the storage of recently used addresses on receipt of a power down command. However, this assertion is not supported by the reference.

That is, at best, Bruce teaches a cache indexing or remapping scheme by which addresses are stored in a backup nonvolatile memory and used after an interruption of power. However, Bruce does not provide a teaching by which a processor issues a power down command and causes a buffer interface to **responsively** store recently used addresses in a nonvolatile memory.

As to Claim 10, note that Bruce does not teach a method including the steps of **detecting of a pending power down and storage**, in a nonvolatile memory, a read address for data buffered in a volatile read buffer.

In short, Bruce does not teach or suggest a system capable of detecting and responding to a pending power loss to enable a rapid recovery as set forth in Claims

10 and 15. Hence, Claims 10, 15, 20 and the Claims dependent thereon should be allowable.

Reconsideration, allowance and passage to issue are respectfully requested.

Respectfully submitted,
Andrew M. Spencer

By _____
William J. Benman
Attorney for Applicant
Registration No. 29,014

Benman, Brown & Williams
2049 Century Park East
Suite 2740
Los Angeles, CA 90067

(310) 553-2400
(310) 553-2675

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200208966-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew M. Spencer

Confirmation No.: 8304

Application No.: 10/609,277

Examiner: Flournoy, Horace

Filing Date: 06/27/2003

Group Art Unit: 2189

Title: NONVOLATILE BUFFERED MEMORY INTERFACE

Mail Stop AF
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

(X) Response/Amendment
( ) New fee as calculated below
( ) No additional fee
( ) Other: _____ (fee $_____)
( ) Petition to extend time to respond
( ) Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	7	MINUS	20	= 0	X $50	$ 0
INDEP. CLAIMS	3	MINUS	5	= 0	X $200	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $360	$ 0
EXTENSION FEE	1ST MONTH $120.00 [ ]	2ND MONTH $450.00 [ ]	3RD MONTH $1020.00 [ ]	4TH MONTH $1590.00 [ ]		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Andrew M. Spencer

By _____
William J. Benman
Attorney/Agent for Applicant(s)
Reg. No. 29,014

Date: 05/29/2007

Telephone No.: (310) 553-2400

(X) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571) 273-8300 on 05/29/2007
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HP 200208966-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Andrew M. Spencer	:	Group Art Unit 2189
Serial No. 10/609,277	:	Examiner: Flournoy, Horace L.
Filed: 06/27/2003	:	Date: May 29, 2007
For: NONVOLATILE BUFFERED	:	
MEMORY INTERFACE	:	

AMENDMENT AFTER FINAL REJECTION

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated April 18, 2007, please consider the following Remarks.

IN THE CLAIMS:

Claims 1 – 9 (Canceled)

10. (Previously Presented) A method of providing access to stored data, the method comprising:

receiving a read command that comprises a read address;

determining whether data from the read address is buffered in a volatile read buffer;

retrieving data from a location in a nonvolatile memory array associated with the read address if the data is not buffered, and buffering the retrieved data in the volatile read buffer;

responding to the read command with data from the volatile read buffers if the data is buffered;

detecting a pending power-down;

storing in nonvolatile memory the read address for data buffered in the volatile read buffer; and

restoring the data to the volatile read buffer when power returns.

11. (Previously Presented) The method of claim 10, wherein said restoring comprises:

accessing the nonvolatile memory to retrieve the read address associated with the read buffer; and

filling the read buffer with data from a memory array, beginning with data associated with the read address.

Claims 12 – 14 (Canceled)

15. (Previously Presented) A digital device that comprises:

a memory having a buffered memory interface with one or more read buffers; and

a processor coupled to the memory device and configured to retrieve stored information from the memory,

said processor being programmed to cause the memory to receive a power down command before electrical power is removed from the memory and the buffered memory interface to responsively store, in a nonvolatile memory, one or more addresses of memory locations that have been recently accessed.

16. (Original) The device of claim 15, wherein the memory interface is further configured to reload the one or more read buffers with data in accordance with information from the nonvolatile memory when power returns.

Claim 17 (Canceled)

18. (Previously Presented) The device of claim 15, wherein the one or more read buffers comprise:

a plurality of read buffers each associated with a different region of the memory and configured to buffer only a subset of data in the associated region for read operations on that region.

19. (Original) The device of claim 18, wherein the memory interface further comprises:

an interface control module that is configured to receive read commands specifying a memory address, wherein the interface control module is coupled to a nonvolatile memory array to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands; and

wherein the memory further comprises:

an error correction code (ECC) decoder coupled between the nonvolatile memory array and the one or more read buffers.

20. (Previously Presented) A system for storing and retrieving data comprising:

means for receiving a read command that comprises a read address;

means for determining whether data from the read address is buffered in a volatile read buffer;

means for retrieving data from a location in a nonvolatile memory array associated with the read address if the data is not buffered, and buffering the retrieved data in the volatile read buffer;

means for responding to the read command with data from the volatile read buffers if the data is buffered;

means for detecting a pending power-down;

means for storing in nonvolatile memory the read address for data buffered in the volatile read buffer; and

means for restoring the data to the volatile read buffer when power returns.